100V N-Channel Enhancement Mode MOSFET

Description

The NP12N10G uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge.It can be used in a wide variety of applications.

General Features

- V_{DS} =100V I_D =12A
  $R_{DS(ON)}$(Typ.)=105mΩ @V_{GS}=10V
  $R_{DS(ON)}$(Typ.)=122mΩ @V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

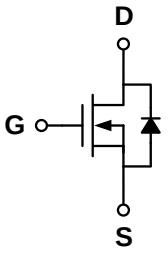
Application

- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package

- TO-252-2L

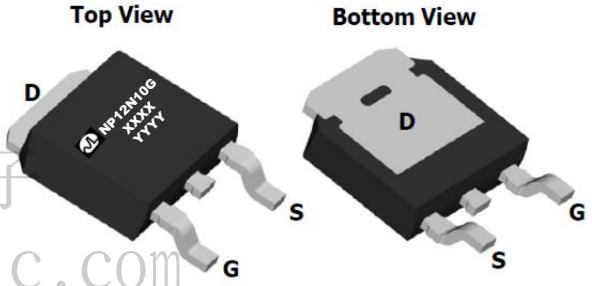
Schematic diagram



Marking and pin assignment

TO-252-2L

（Top View）



NP12N10G—Product Name

XXXX—Wafer Lot No.

YYYY—Date Code

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP12N10G-G	-55°C to +150°C	TO-252-2L	2500

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	±20	V
Continuous Drain Current	TC=25°C	I_D	12	A
	TC=100°C		8	
Pulsed Drain Current		I_{DP}	48	A
Avalanche energy(L=0.5mH) (note1)		E_{AS}	25	mJ
Maximum power dissipation	TC=25°C	P_D	50	W
Operating junction Temperature range		Tj	-55—150	℃

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Static Characteristics							
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA		100	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=100V, $_{GS}$=0V	T_J=25°C	-	-	1	μA
			T_J=85°C	-	-	30	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V		-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA		1	1.6	2.5	V
Drain-source on-state resistance[1]	$R_{DS(ON)}$	V_{GS}=10V, I_D=12A		-	105	130	mΩ
		V_{GS}=4.5V, I_D=10A		-	122	150	
On Status Drain Current	$I_{D(ON)}$	V_{DS}=100V, V_{GS}=10V		12	-	-	A
Diode Characteristics							
Diode Continuous Forward Current	I_S			-	-	12	A
Reverse Recovery Time	t_{rr}	I_F=12A, dI/dt=100A/us		-	22	-	ns
Reverse Recovery Charge	Q_{rr}			-	90	-	nC
Dynamic Characteristics[2]							
Input capacitance	C_{ISS}	V_{GS}=0V ,V_{DS}=50V f=1.0MHz		-	830	-	pF
Output capacitance	C_{OSS}			-	44.2	-	
Reverse transfer capacitance	C_{RSS}			-	23	-	
Turn-on delay time	$t_{D(ON)}$	V_{GS}=10V, V_{DD}=50V, I_D=12A		-	15	-	ns
Turn-on Rise time	tr			-	5	-	
Turn-off delay time	$t_{D(OFF)}$			-	25	-	
Turn-off Fall time	tf			-	7	-	
Total gate charge	Q_g	V_{GS}=10V,I_D=12A V_{DS}=50V		-	22.3		nC
Gate-source charge	Q_{gs}				2.87		
Gate-drain charge	Q_{gd}			-	6.14	-	
Drain-Source Diode Characteristics							
Diode forward voltage	V_{SD}	I_{SD}=12A,V_{GS}=0V		-	0.8	1.1	V

Note: 1：Eas test：VDD=50V，RG=50ohm，L=500uH

2：Pulse test; pulse width ≦ 300ns, duty cycle ≦ 2%.

3：Guaranteed by design, not subject to production testing.

Figure A: Gate Charge Test Circuit & Waveforms

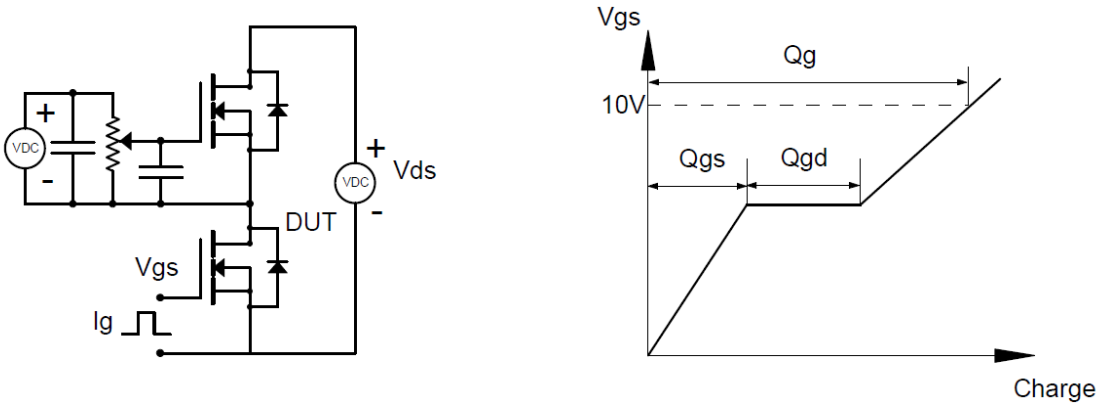


Figure B: Resistive Switching Test Circuit & Waveforms

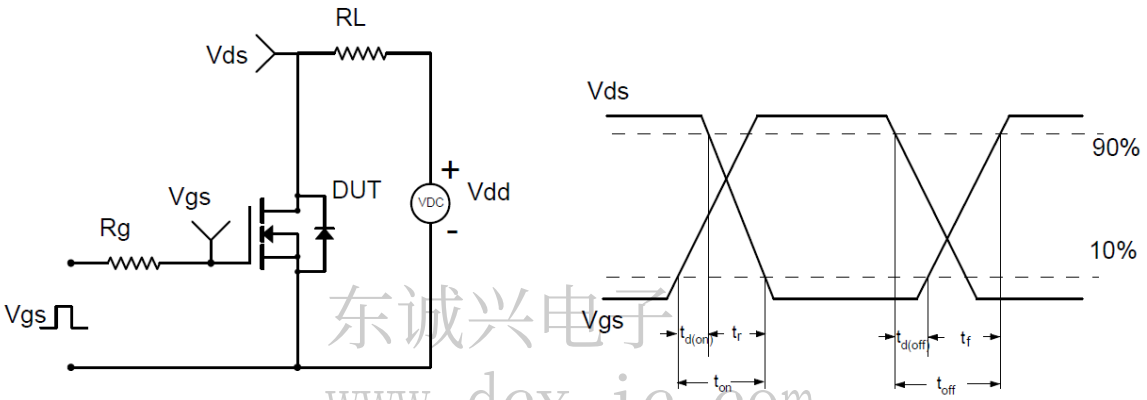


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

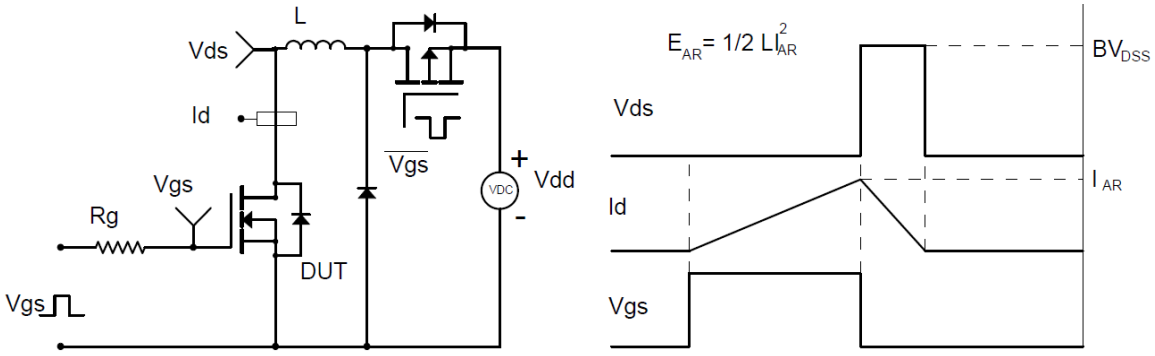
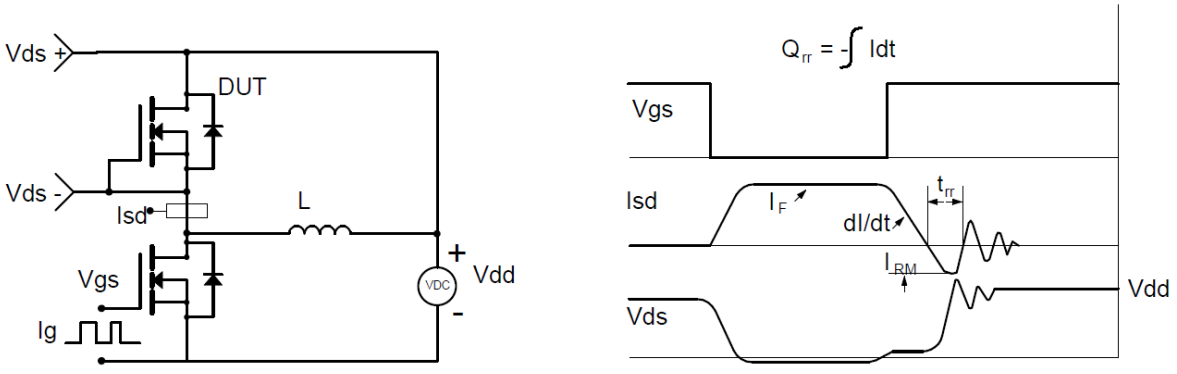
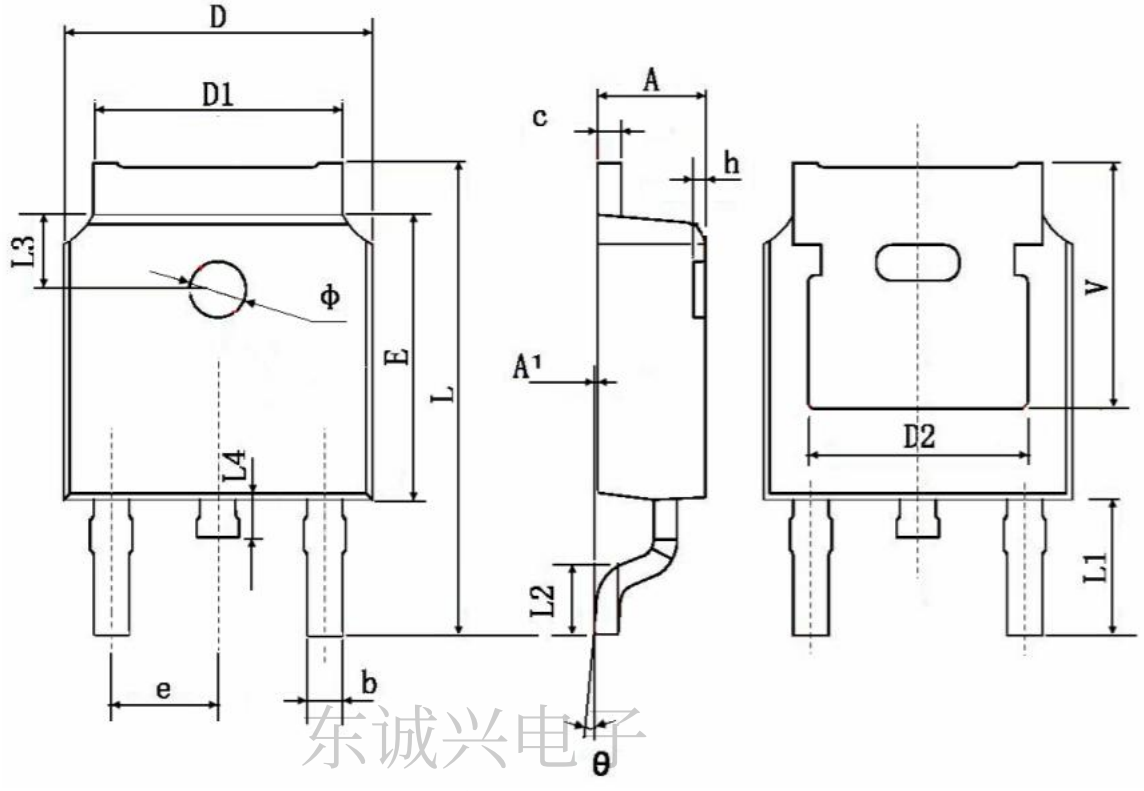


Figure D: Diode Recovery Test Circuit & Waveforms



Package Information

- **TO-252-2L**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	